Here are the architecture that Mos 1.0 currently covers(Have Mos 1.0 and Software for all of this architectures) !!!

- Mos32 and Mos64: (included Intel architecture amd, amd64 and Intel based Mac OSX), NB: since 01-01-2006 all Mac OSX are Intelbase
- Mos390: S390 (Main Frames architecture),
- MosIntosh: Mac OSX (PPC),NB All Mac OSX build before 31-12-2005 are PowerPC or PPC
- MosARM: ARM
- MosSPARC: SPARC

Mos32 and Mos64: (included Intel architecture amd, amd64 and Intel based Mac OSX), most computers used based on this !!!

S/390 &□□ ESA/390 (Enterprise Systems Architecture/390) Was Introduced in September 1990 [1] and IS IBMâ□□s last mainframe 31-bit-address/32-bit-data computing design, copied by Amdahl, Hitachi, and Fujitsu Among Other Competitors. It Was the Successor of System/370 and has-been by the SUCCEEDED 64-bit z / Architecture in 2000. Machines Have Been Supporting the architecture sold from under the brand System/390 (S/390) from The Beginning of the 1990s. The 9672 implementations of System/390 Were the first high-end IBM mainframe architecture Implemented first with CMOS CPU electronics Rather Than the traditional bipolar logic.Computing1

PowerPC, sometimes abbreviated PPC, is a family of microprocessors derived from POWER RISC processor architecture of IBM, and developed jointly by Apple, IBM and Freescale (formerly Motorola Semiconductors). The reverse acronym for PowerPC Performance Optimization With Enhanced is RISC Performance!

ARM platforms supported Out of the box, ARM Mos officially supports two systems: ARM Versatile platform (via QEMU emulator) Marvell SoC (System on Chip), including: SheevaPlug (original & eSATA) GuruPlug OpenRD based, client and Ultimate. Minimum target CPU Starting with Mos ARM 1.0, the packages are compiled for the target at least: ARMv4t Little Endian Softfloat EABI (version 4 +) This means that user-space works on most ARM devices on the market today.

SPARC Jump to: navigation, search SPARC The SPARC processor architecture is open. ***SPARC***
is the reverse acronym for Scalable Processor Architecture (
scalable processor architecture
). It is RISC, favoring pipeline reduced instruction set. This architecture supports in 1995 and addresses the data memory 64-bit. The first SPARC microprocessors were developed at Berkeley in 1984. The evolution of the architecture is decided by SPARC International, grouping including Sun Microsystems, Fujitsu and Texas Instruments. There are three versions of this architecture: SPARC V7: appeared around 1987, 32-bit architecture SPARC V8 appeared around 1991, 32-bit architecture SPARC V9: appeared around 1994, 64-bit architecture SPARC is an architecture whose specifications are free, providing the freedom for anyone to create a compatible processor. A processor uses the completely free SPARC V8 instruction set: the LEON. It is licensed under the LGPL by the FSF. The SPARC V7 also led the development of the ERC32 processor, radiation tolerant and used in space.